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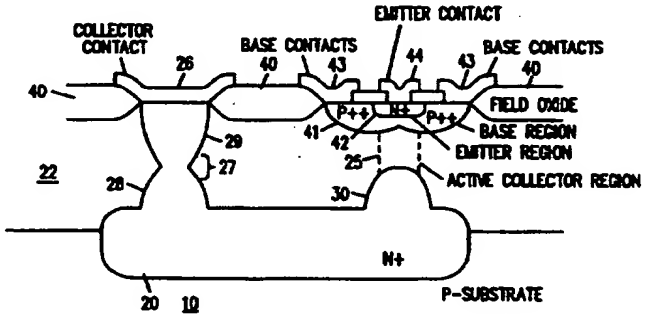

(57) Abstract

A method of fabricating bipolar transistors with low collector resistances uses the high density implantation of higher diffusivity dopants into the buried collector layer (20). A more lightly doped epitaxial layer (22) is then grown which will form the active collector region. During the heat cycle of the epitaxial growth, the higher diffusivity dopants up-diffuse into the overlying epitaxial active collector layer, thus decreasing the effective thickness of the active collector region. If the buried layer (20) and the high diffusivity sinker-up regions (28, 30) are implanted with separate masks, the sinker-up region can be restricted to the area beneath the area where the base (41) and emitter (42) will subsequently be formed, thus minimizing any increase in collector capacitance. After the base (41) and emitter (42) are implanted into the epitaxial layer, the thickness of the lightly doped epitaxial layer between the base and the up-diffused highly doped sinker-up region (30) is less than the thickness from the base (41) to the buried layer in the absence of a sinker-up region. Less distance translates into lower resistance and lower breakdown voltage. Since a separate mask is used to implant the sinker-up, the sinker-up can be excluded in any of the transistors; thus, both high and low resistance devices can be simultaneously fabricated on the same chip. If the same mask is used to implant the up-diffusion and the buried layer, a two-step active collector doping profile can be realized without using two separate epitaxial growths, and without adding any additional masks.

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LOW COLLECTOR RESISTANCE BIPOLAR TRANSISTOR COMPATIBLE WITH HIGH VOLTAGE INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to bipolar transistor and process technologies. Particularly, this invention relates to device structures and processes compatible with high-voltage integrated circuits. This invention addresses the need for making low collector resistance and high breakdown voltage devices on the same die and making less costly low resistance devices.

2. DESCRIPTION OF RELATED ART

In order to achieve high-voltage operation while avoiding transistor breakdown, a collector region with a low doping level and large thickness must be used. Unfortunately, when such a transistor is operated at low collector-emitter voltages, this results in the undesirable consequence of high collector resistance. The resistance occurs because at low voltages, the depletion region on the collector side of the collector-base junction does not extend very far into the active collector region. Therefore, the current must travel to the buried collector layer through the large remaining distance facing high resistance per unit distance of the lightly doped active collector region.

The resulting high collector resistance causes the early onset of saturation. Early saturation occurs because an internal voltage drop occurs from the collector contact to the collector-base junction due to the high collector resistance. This internal voltage drop may exceed the voltage applied across the collector and emitter terminals. This type of saturation caused by an internal voltage drop is called quasi-saturation.

In high-voltage integrated circuits, not all of the transistors operate over the full supply voltage. For example, the collector-base voltage of the common-emitter transistor in a cascode amplifier is generally much less than the power supply voltage. If this reduced collector-base voltage becomes small enough, quasi-saturation may occur. Therefore, for optimized performance, it is desirable to minimize the quasi-saturation effects. Often, these devices which will normally operate at less than the full supply voltage also do not need to meet the higher breakdown voltage specification that the other higher-voltage devices on the chip must meet, because the risk of breakdown decreases with the decreased supply voltage. At least for the devices in the circuit which do not have to require the full breakdown voltage specification, it is desirable to minimize the quasi-saturation effects.

Figure 1 is an example of a typical bipolar NPN transistor configuration. A highly doped N+ buried layer is connected to the collector contact and is used to provide a low resistance path to the overlying moderately or lightly doped N-type active collector region which is adjacent to the base. The P-type base region lies on top of the collector, and the N-type emitter region lies on top of the base. Since the conductivity of a doped semiconductor region increases with the magnitude of doping concentration, the more highly doped N+ buried layer has less resistance per unit distance than the N-type active collector region. Thus, the overall internal collector resistance as measured from the collector contact to the collector-base junction is largely governed by the resistance encountered through the highly resistive N-type active collector region. One way to reduce this resistance is by reducing the distance from the N+ buried region to the base by decreasing the thickness of the N-type active collector region.

When the thickness of the active collector region is decreased, the overall internal collector resistance decreases; however, the breakdown voltage of the device also decreases, at least in the most common situations in which the breakdown voltage is governed by the thickness of the active collector region rather than the minimum radius of curvature of the extrinsic base. Thus, a design tradeoff occurs between the breakdown voltage and the internal collector resistance and is adjusted by varying the thickness of the active collector region.

In many integrated circuits (such as the cascode amplifier mentioned above), it is desirable both to have devices with high-resistance collectors and high breakdown voltages and also to have devices with flower-resistance collectors and lower breakdown voltages on the same chip. The present invention accomodates such a desire. With the present invention, collectors can be defined to have high resistance or to have low resistance on a transistor by transistor basis, such that the desired collector resistance is entirely independent of the location of the transistor on the chip. Using the present invention, no high resistance or low resistance areas on the chip need to be defined; rather, high resistance and low resistance transistors can be thoroughly mixed together in their placements on the chip. No prior art has been located which attempts to allow for the manufacture of high resistance and low resistance collectors on the same chip, even when such distinct transistors are segregated into separate, distinct areas of the chip. Figure 2 is a simplified illustration of a conventional higher collector resistance transistor positioned next to a lower collector resistance transistor made according to the present invention. The low collector resistance transistor has a small region of highly doped N+ material beneath the base and emitter regions which reduces the thickness (W_t) of the active collector region in the region where the current flows, thus decreasing the collector resistance for that transistor.

Prior engineering efforts have used structures which are somewhat similar to structures constructed according to the present invention. However, these efforts accomplished different objectives, and do not accomplish the objectives of the present invention. Furthermore, the resulting structures were different from the presently proposed structures.

For example, a selectively ion-implanted collector (SIC) device is depicted in Figure 3A. See Konaka, et al., Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 331-334. SIC processes are generally used to produce low voltage, high current density devices. The SIC implantation is not used to reduce the collector resistance. Rather, SIC is used to increase the collector doping at the base-collector junction such that higher current densities can be achieved, while minimizing the collector-base capacitance. SIC is usually carried out at the emitter opening step. Once the emitter area is defined, a high energy implant is carried out to add dopant under the emitter, near the collector-base junction. This technique cannot be used to reduce the collector resistance of high-voltage devices because it is impossible to implant down through the collector to the buried layer junction.

This SIC type of implant would not be useful for thick epitaxial processes since the region from the SIC implant peak to the buried layer would remain doped at a low level. Therefore, the collector would remain highly resistive. The doping profile for a SIC device is depicted in Figure 3B. Note that the SIC implantation occurs right at the collector-base junction.

For high voltage transistor operation such as is desired in the present invention, the N+ region must be located much further away from the collector-base junction to avoid breakdown at higher voltages. The SIC implant is not helpful in reducing the collector resistance because it is very shallow in comparison to the thickness of the lightly-doped N- region. More importantly, the SIC implant radically changes the characteristics of the transistor. Indeed, this change in the characteristics of the device is the

purpose for using the SIC implant. The SIC implant reduces the base width, reduces the net base doping concentration, increases the collector doping at the collector-base junction, increases the current density, and decreases the gain of the device; in contrast, using the present invention, it is desired that none of these transistor characteristics be affected. Thus, the SIC method alters many of the important transistor parameters such as gain. Alternatively, using the present invention, an objective is to maintain equality of the device parameters for the low collector resistance devices and the high collector resistance devices which can exist on the same chip.

Epitaxial growth of a lightly doped active collector region on top of a heavily doped substrate is a common in the semiconductor processing industry. See, for example, S. M. Sze, Physics of Semiconductor Devices, 2nd Ed., John Wiley & Sons, Inc., p. 146, Fig. 10, 1981. Figure 4A depicts the doping profile for a typical NPN transistor in which the active collector was created by epitaxial growth.

Another commonly used process which results in two separate doping levels for the active collector region involves double epitaxial growth. See, for example, D. J. Roulston, Discrete Bipolar Semiconductor Devices, McGraw-Hill Press, pp. 297-301, and p. 298, Figure 12.5, 1990. Figure 4B depicts a doping profile which might result from such a double epitaxial growth process. This process is generally used in the fabrication of High Power Discrete Transistors. This dual collector doping process is used to improve the high current switching behavior of the device. Figure 4C is a simplified illustration of a typical NPN bipolar structure built by double epitaxial growth which might have the doping profile shown in Figure 4B.

In a modern bipolar transistor with a lightly doped epitaxial collection region, the current gain is affected by the relocation of the high-field region from point A on Figure 4A to point B on Figure 4A. The effective base width increases from W_b to $(W_b + W_c)$. This base widening effectively decreases the gain because the magnitude of the gradient of the free electron density decreases as the base widens.

The bottom epitaxial layer is more highly doped than the upper epitaxial layer, as shown in Figure 4B. The purpose of this disparity is to minimize base widening effects when the device is operated at high current levels. By using a transistor having a collector with a two-step collector concentration gradient, the amount of base widening can be decreased by the thickness of the second layer.

Since epitaxial techniques are used in the double epitaxial collector process, it is not possible to realize high and low resistance devices on the same die. The active collector thicknesses for all the transistors will be equal. Additionally, this process is costly since it requires two separate epitaxial growths for the two separate layers.

SUMMARY OF THE INVENTION

In order to achieve high-voltage operation for bipolar transistors, collector regions with low doping levels and large thicknesses must be used. These usages result in high collector resistance when the collector-emitter voltage is too low to fully deplete the collector. This high collector resistance results in the early onset of saturation. An internal voltage drop results from the high collector resistance, and this voltage drop may exceed the voltage applied at the terminal voltages. This is referred to as quasi-saturation. In high-voltage circuits, not all transistors operate over the full voltage. For example, the collector-base voltage of the common-emitter transistor in a cascode amplifier is generally much less than the power supply voltage. Therefore, for optimized performance, it would be desirable to minimize the quasi-saturation effects, at least for the devices which do not require the full breakdown voltage specification.

The present invention includes transistor structures and methods for producing them. The methods for producing them involve the use of high concentrations of fast-diffusing dopants implanted in the buried collector layer to diffuse upwardly into the active collector region. In order to reduce the collector contact or collector sinker resistance, sinker-up and sinker-down diffusions are used to connect the buried collector layer to the surface contact. If the sinker-up diffusion is located under the emitter, the effective active collector thickness is reduced, and the collector resistance is in turn reduced. Therefore, no extra masks or processing steps are needed if the sinker-up is already required in the process to connect to the contact.

One embodiment of the present invention reduces the thickness of the active collector, but only in the area directly below the base and emitter. Because this active collector thickness reduction is caused by selectively including or not including a sinker-up region beneath the emitter, both high resistance and low resistance devices can be developed on the same die. This embodiment also minimizes the increase in capacitance caused by reducing the effective collector thickness by restricting the area of reduced collector thickness to the area beneath the emitter region, where essentially all the current will flow.

Another embodiment of the present invention specifies the manufacture a transistor with a two-step active collector profile. In that embodiment, however, reduced active collector thickness extends across the entire length of the buried layer, because the same mask is used to implant the up-diffusion dopant as is used to implant the buried layer. The novelty of this embodiment stems not only from the fact that the two step profile is a result of the up-diffusion into a single epitaxial layer, whereas prior art methods have utilized more expensive double epitaxial layers, but also that a separate sinker-up implantation mask can be saved since it is not needed.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description of the invention and accompanying drawings which set forth illustrative embodiments in which the principals of the invention are utilized.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified cross-sectional drawing of a typical prior art bipolar NPN transistor configuration.

Figure 2 is a simplified cross-sectional drawing of a high collector resistance transistor and a low collector resistance transistor constructed next to each other as in a first embodiment of the present invention.

Figure 3A is a cross-sectional drawing of a prior art NPN transistor utilizing a Selectively Ion-Implanted Collector (SIC) process.

Figure 3B is a net doping concentration profile for the prior art SIC transistor shown in Figure 3A.

Figure 4A is a net doping concentration profile for a typical prior art NPN transistor with a single epitaxial layer active collector.

Figure 4B is a net doping concentration profile for a typical prior art NPN transistor with a double epitaxial layer active collector.

Figure 4C is a cross-sectional drawing of a typical prior art NPN transistor with a double epitaxial layer active collector.

Figure 5 is a cross-sectional drawing of the buried layer collector formation according to the present invention.

Figure 6 is a cross-sectional drawing of the formation of the sinker-up region according to the first embodiment of the present invention.

Figure 7 is a cross-sectional drawing of the epitaxial growth of the active collector region according to the present invention.

Figure 8 is a cross-sectional drawing of the formation of the sinker-down region according to the present invention.

Figure 9 is a cross-sectional drawing of an entire NPN bipolar transistor with low collector resistance fabricated according to the first embodiment of the present invention.

Figure 10 is a cross-sectional drawing of a higher resistance and a lower resistance transistor placed side by side, with both devices fabricated according to the first embodiment of the present invention.

Figure 11 is a cross-sectional drawing of an entire NPN bipolar transistor with low collector resistance fabricated according to a second embodiment of the present invention.

Figure 12 is typical net doping concentration profile for the transistor of Figure 11.

DETAILED DESCRIPTION OF THE INVENTION

Figures 5 through 9 illustrate the steps for fabricating an NPN low collector resistance transistor according to a first embodiment of the present invention. Figure 9 depicts a completed bipolar structure manufactured according to that embodiment. This embodiment allows the simultaneous manufacture of high resistance transistors and low resistance transistors on the same die. Using a standard vertical NPN configuration according to this embodiment, the high-resistance transistors might have a breakdown voltage of 85 volts, and the low-resistance transistors might have a breakdown voltage of 40 volts. To achieve breakdown voltages this high, thick epitaxial layers must be used to create the active collector region. In situations in which the breakdown voltage is governed by the minimum radius of curvature of the extrinsic base region rather than the active collector thickness, the low collector resistance transistors may have the same breakdown voltage as the higher collector resistance transistors.

To reduce the collector contact series resistance, collector sinkers are used to highly dope the region between the top surface and the buried layer. Both N+ sinker-down and N+ sinker-up implants and diffusions are used to reduce the vertical collector contact resistance. The down and up diffusions are similar to the isolation up and down diffusions generally used in junction isolated processes.

Referring to Figure 5, the fabrication process begins with a silicon substrate 10 of P-type conductivity. Typically, the P-type substrate will have been developed as an isolation well for the NPN type devices which will reside on that section of the chip. A typical doping concentration for the substrate is approximately 2×10^{15} atoms per cm^3.

A buried layer implantation mask 11 is developed as shown in Figure 5. The dopant used in the implantation to create the N+ buried layer 20 is typically a slow diffusing N-type element such as Antimony (Sb) or Arsenic (As). For instance, an implantation of Arsenic followed by a high temperature diffusion cycle might be conducted to result in a junction depth of approximately 4 microns, such that the peak concentration is approximately 5×10^{18} atoms per cm^3.

As illustrated in Figure 9, this N+ buried region 20 will eventually serve as a low resistance path through the active collector region 25 that is part of an epitaxial layer 22 which will be grown above the buried layer 20. To provide continuity between the collector contact 26 and the N+ buried layer 20, a low resistance vertical region 27 will be constructed using N+ sinker-up region 28 and N+ sinker-down regions 29. The sinker-down region 29 and the sinker-up regions 28 and 30 are formed using a dopant which has a faster diffusion rate than that of the dopant used to form the buried layer 20.

Referring again now to Figures 5 and 6, following the ion implantation of the N+ buried layer 20, an annealing process can be performed to drive the dopant and to repair implantation damage. After this

optional drive step, the sinker-up mask 12 needs to be formed. Although it is possible to strip the mask 11 which was used to perform the buried layer implantation before defining the sinker-up mask 12, it is unnecessary to perform this removal. Since the N+ sinker-up regions 28 and 30 will always be implanted within the N+ buried layer 20, the previous mask may remain in place and a new mask oxide layer 12 can be formed on top of the old one. Figure 6 shows a sinker-up oxide mask 12 which was formed on top of the previous buried layer mask 11, as indicated by the varying thickness of the mask oxide 12.

The N+ sinker-up region is then formed by implanting a faster diffusing N-type dopant such as Phosphorus (P) into surfaces of the buried layer exposed by the implantation mask 12. After this implantation, the mask oxide 12 is stripped away.

Referring to Figure 7, now that the sinker-up regions 28 and 30 are defined, an N-type epitaxial layer is grown having a dopant concentration of approximately 10^{15} atoms per cm^3. Figure 7 shows the resulting structure at the end of this growth. The thermal cycle inherent in the epitaxial growth cycle will cause the N+ buried layer 20 and the N+ sinker-up regions 28 and 30 to up-diffuse as well as anneal damage caused by the N+ sinker-up implantation. The N+ regions beneath the epitaxial layer 22 have diffused upward into the epitaxial layer 22 as shown in Figure 7. Because the N+ sinker-up regions 28 and 30 were implanted with a higher diffusivity dopant than the dopant used to form the N+ buried layer 20, the sinker-up regions 28 and 30 have diffused further into the epitaxial layer 22.

Figure 8 shows the formation of the N+ sinker-down region 29. After the epitaxial growth, a mask 31 is created specifically for the implantation of the sinker-down region. Since the sinker-down region 29 is designed to diffuse downward into the sinker-up region 28, the N+ sinker-down region 29 is implanted with a faster diffusing material such as Phosphorus (P). The sinker-down region 29 is driven such that the desired diffusion occurs. The dotted lines in Figure 8 show the location of the sinker-down region after the drive cycle causes diffusion. Since the sinker-down and sinker-up locations are overlapping after the sinker-down diffusion, there is continuity from the buried layer to the collector contact shown in Figure 9.

The remaining steps of the transistor fabrication are of the standard variety, and the finished NPN bipolar transistor is shown in Figure 9. Field oxide areas 40 are formed; the base region 41 and emitter region 42 are formed; the terminals are covered with polysilicon contacts 43 and 44; and those contacts 43 and 44 are metalized (not shown). When completed, a typical structure might appear as shown in Figure 9.

The transistor of Figure 9 is an NPN bipolar transistor with low collector resistance. Since the process already uses one mask (12 in Figure 6) and implant step to create the sinker-up region 28 used to connect the collector contact 26 and the buried layer 20, there is no extra cost involved with simultaneously providing the low-resistance option by implanting the sinker-up region 30 beneath the emitter 42. Two base contacts 43 are shown on Figure 9 to reduce base resistance, although double base contacts are not required to practice the present invention. The dotted lines in Figure 9 indicate the active collector region 25. Almost all of the collector current will travel in this region.

It is worth noting that the size of the openings in the N sinker-up mask is not necessarily related to the width of the emitter. Because the N sinker-up region 30 diffuses sideways as well as vertically, the implantation in Figure 6 may be narrower than the emitter in order to minimize capacitance while still lowering the resistance. Alternatively, the N sinker-up region 30 implanted may be wider than the emitter as well.

Figure 10 illustrates a higher resistance transistor 50 and a lower resistance transistor 60 formed next to each other. With one exception, the higher resistance transistor 50 on the left was formed by an

identical process as the lower resistance transistor 60 on the right. The only difference is that the transistor 50 shown on the left of Figure 10 does not include a sinker-up region 30 beneath the emitter 42 and base 41. Instead, the sinker-up mask (12 in Figure 6) did not provide a gap in that region, and thus no ions were implanted in the area beneath the emitter 42 and base 41 of that transistor 50.

For the higher resistance transistor 50, the distance from the N+ collector buried layer 20 to the P-type base region is greater than the distance from the N+ sinker-up region 30 to the P-type base region 41 for the lower resistance transistor 60 shown on the right. Since all the other parameters of the two transistors are the same, the high-resistance transistor 50 and low-resistance transistor 60 will have nearly identical gains and other characteristics. The only differences will be the collector resistances, the breakdown voltages, and the collector capacitances.

Referring again to Figure 9, when the more highly doped diffusion area 30 is placed more closely to the base region 41, the collector capacitance increases. Since the more highly doped N+ diffusion region 30 holds more charge than the less doped epitaxial layer 22, and that charge is positioned closer to the base 41, the base-collector capacitance increases.

A great advantage of this embodiment of the present invention as shown in Figure 9 is that the capacitance increase caused by decreasing the collector resistance is minimized since the sinker-up region beneath the emitter is closer to the base only in the region where the current will flow.

A second embodiment of the present invention allows the fabrication of lower resistance devices without requiring a separate sinker-up mask. Figure 11 depicts an NPN bipolar transistor manufactured according to this second embodiment of the present invention. Since there is no separate sinker-up mask (12 in Figure 6), the higher diffusivity N-type dopant such as Phosphorus (P) can be implanted simultaneously with the lower diffusivity N-type dopant such as Antimony (Sb) or Arsenic (As) using the N+ buried layer mask (11 in Figure 5). If the two implantations are done simultaneously, the two different types of dopants penetrate the substrate to approximately the same depth. When the heat cycle then occurs during the epitaxial growth, the Phosphorus (P) and the Antimony (Sb) will diffuse both upwardly and downwardly. Since the Phosphorus (P) diffuses faster, the N+ up-diffusion region 35 will extend above and below the diffused buried layer 20, as shown in Figure 11.

Figure 12 shows a typical net dopant concentration profile for the structure of Figure 11. The concentration in the up-diffused collector region 35 does not affect the gain of the transistor. This concentration can be adjusted to be higher or lower without affecting the device parameters other than the breakdown voltage, collector resistance, and the collector-base capacitance.

Alternatively, the higher diffusivity dopant can be implanted before or after the lower diffusivity dopant. If the higher diffusivity dopant is implanted prior to or subsequent to the lower diffusivity buried layer implant, the implantation energy of the high diffusivity dopant can be reduced so that the down diffusion into the substrate is minimized.

While this second embodiment of the present invention shown in Figure 11 is less expensive and less complicated than the first embodiment shown in Figure 9, this cost savings is traded off against other factors. In Figure 11, since the up-diffusion region 35 extends all along the entire width of the N+ collector buried layer 20, the distance between the base and the up-diffusion is reduced throughout the entire width of the base 41, not only in the region where current flows. This increases the size of the capacitance between the base 41 and the collector 35, thus reducing the upper limit of the operation frequency of the transistor at least to some extent.

Since the same mask (11 in Figure 5) is used to implant the N+ buried layer 20 and the N+ up-diffusion 35, it is impossible to selectively produce high resistance transistors and low resistance

transistors on the same chip. All transistors must either be implanted with the N+ up-diffusion or not implanted since no additional mask is provided to select which collectors are shielded from the up-diffusion implant. However, this process has the advantage that a two-step buried layer collector doping profile such as the one shown in prior art Figure 4B can be produced without using two epitaxial growth cycles.

Figure 12 shows a typical net doping concentration profile for an NPN bipolar transistor made according to this second embodiment of the present invention. The similarity in prior art Figure 4B and Figure 12 is evident. The N+ up-diffusion (35 in Figure 11) provides an intermediate level of doping in the collector region. Among other reasons, this is useful to control base widening effects.

While accomplishing the same end result, the present invention shown in Figure 11 is superior to that of prior art Figure 4C because only one epitaxial growth is required rather than two. Furthermore, the prior art double epitaxial growth process cannot be used to make high-resistance transistors and low-resistance transistors on the same chip.

An additional benefit that is available using either embodiment of the present invention is that the doping profiles of NPN and PNP devices fabricated on the same wafer can be made more similar. Adding the more quickly diffusing N-type dopant to the buried layer of the NPN transistors can be used to increase the diffusivity level of the N+ collector to about the same level as the diffusivity of the P-type dopant used to form the P+ buried layer collector regions of the PNP devices. Reducing the difference in upward diffusivity of the collectors of the NPN-type and PNP-type transistors facilitates effective complementary bipolar process optimization.

While previously described in the context of NPN-type devices, of course the embodiments previously described also apply equally well to PNP-type devices. Typically, Boron (B) could be used as the slower diffusing P-type dopant used to create the P+ buried collector layer. For the fast diffusing P+ sinker-up regions, Aluminum (Al) is a suitable P-type dopant.

The use of the up-diffused collector embodiments according to the present invention has been discussed in the context of complementary bipolar circuits in which only the NPN devices employ the up-diffusion techniques to facilitate process optimization. However, it should be noted that the up-diffused collector embodiments according to the present invention can also be implemented in bipolar processes in which only the PNP devices employ the up-diffusion techniques, or in which both the NPN and the PNP devices use the up-diffused collector techniques. In order to implement complementary bipolar processes, an N-well must simply be added in the P-substrate to isolate the PNP buried layers form the P- substrate.

While the present invention has been disclosed above with particular reference to the preferred embodiments shown, those embodiments are presented by way of example, not by way of limitation. Those of ordinary skill in the art would be enabled by this disclosure to add to or modify these embodiments of the invention in various ways as neeeded and still be within the scope and spirit of the present invention as recited in the appended claims.

What is claimed is:

1. A method of fabricating a bipolar transistor having a reduced active collector thickness in the region directly beneath a base and an emitter, the method comprising steps of:

(a) forming a first collector region having a first dopant concentration by implanting first doping ions of the first conductivity type having a first diffusion rate into a substrate of a second conductivity type;

(b) forming a sinker-up region within a portion of the first collector region by implanting second doping ions of the first conductivity type having a second diffusion rate which is greater than the first diffusion rate;

(c) forming a second collector region by epitaxially growing on the substrate a layer of material of the first conductivity type having a second dopant concentration which is less than the first dopant concentration, such that the epitaxial growth process has a thermal cycle which causes the sinker-up regions to diffuse upwardly;

(d) forming a base region by implanting ions of a second conductivity type to a first depth into the epitaxial layer directly above a sinker-up region; and

(e) forming an emitter region by implanting ions of a first conductivity type to a second depth which is less than the first depth into the base region directly above the sinker-up region.

2. A method as in claim 1 further comprising before step (a), a step of oxidizing the surface of the substrate.

3. A method as in claim 1 further comprising after step (a), a step of annealing the first collector region.

4. A method as in claim 1 wherein the first conductivity type is N-type and the second conductivity type is P-type.

5. A method as in claim 1 wherein the first conductivity type is P-type and the second conductivity type is N-type.

6. A method as in claim 4 wherein the first doping ions are either Antimony (Sb) or Arsenic (As).

7. A method as in claim 4 wherein the second doping ions are Phosphorus (P).

8. A method as in claim 5 wherein the first doping ions are Boron (B).

9. A method as in claim 5 wherein the second doping ions are Aluminum (Al).

10. A method of fabricating a bipolar transistor having a reduced active collector thickness, the method comprising steps of:

(a) forming a first collector region having a first total dopant concentration by implanting first doping ions of the first conductivity type having a first diffusion rate and a first ion concentration and implanting second doping ions of the first conductivity type having a second diffusion rate which is greater than the first diffusion rate and a second ion concentration into a substrate of a second conductivity type;

(b) forming a second collector region by epitaxial growing on the substrate a layer of material of the first conductivity type having a second total dopant concentration which is less than the first total dopant concentration, such that the epitaxial growth has a thermal cycle which causes the implanted first and second doping ions in the first collector region to diffuse upwardly into the epitaxial layer such that the second doping ions diffuse further up into the epitaxial layer than the first doping ions;

(c) forming a base region by implanting ions of a second conductivity type to a first depth into the epitaxial layer; and

(d) forming an emitter region by implanting ions of a first conductivity type to a second depth which is less than the first depth into the base region.

11. A method as in claim 10 further comprising before step (a), a step of oxidizing the surface of the substrate.

12. A method as in claim 10 further comprising after step (a), a step of annealing the first collector region.

13. A method as in claim 10 wherein the first conductivity type is N-type and the second conductivity type is P-type.

14. A method as in claim 10 wherein the first conductivity type is P-type and the second conductivity type is N-type.

15. A method as in claim 13 wherein the first doping ions are either Antimony (Sb) or Arsenic (As).

16. A method as in claim 13 wherein the second doping ions are Phosphorus (P).

17. A method as in claim 14 wherein the first doping ions are Boron (B).

18. A method as in claim 14 wherein the second doping ions are Aluminum (Al).

19. A bipolar transistor, having a reduced active collector thickness in the region directly beneath a base and an emitter, comprising:

(a) a buried collector region of a first conductivity type having a first dopant concentration;

(b) a sinker-up region of the first conductivity type having a second dopant concentration which protrudes upward from the buried collector only in the region which is below the emitter;

(c) an active collector region of the first conductivity type having a third dopant concentration above the buried collector and sinker-up regions;

(d) a base region of a second conductivity type above the active collector region; and

(e) an emitter region of the first conductivity type above the base region.

20. A bipolar transistor as in claim 19 wherein the first conductivity type is N-type and the second conductivity type is P-type.

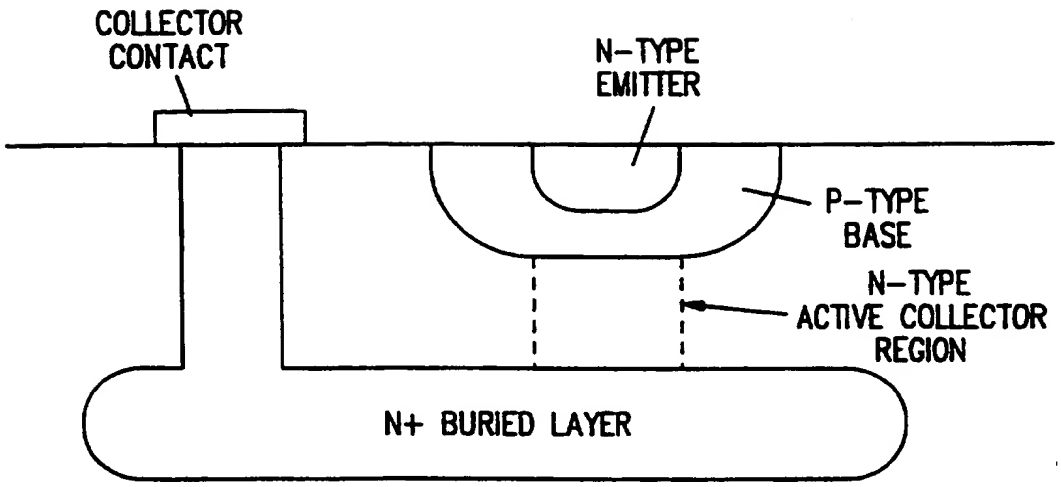
21. A bipolar transistor as in claim 19 wherein the first conductivity type is P-type and the second conductivity type is N-type.

22. A bipolar transistor as in claim 20 wherein the first dopant is either Antimony (Sb) or Arsenic (As) ions.

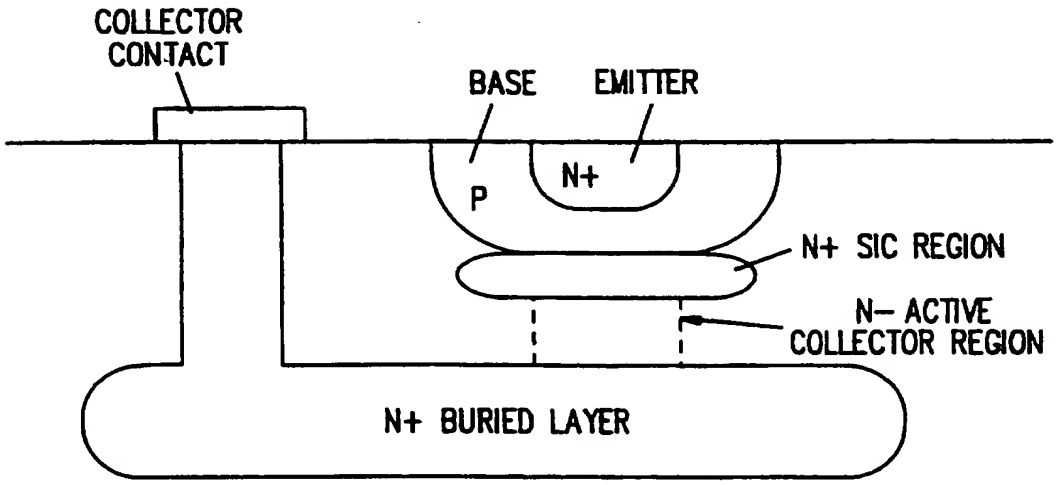
23. A bipolar transistor as in claim 20 wherein the second dopant is Phosphorus (P) ions.

24. A bipolar transistor as in claim 21 wherein the first dopant is Boron (B) ions.

25. A bipolar transistor as in claim 21 wherein the second dopant is Aluminum (Al) ions.



PRIOR ART
FIG. 1



PRIOR ART
FIG. 3A

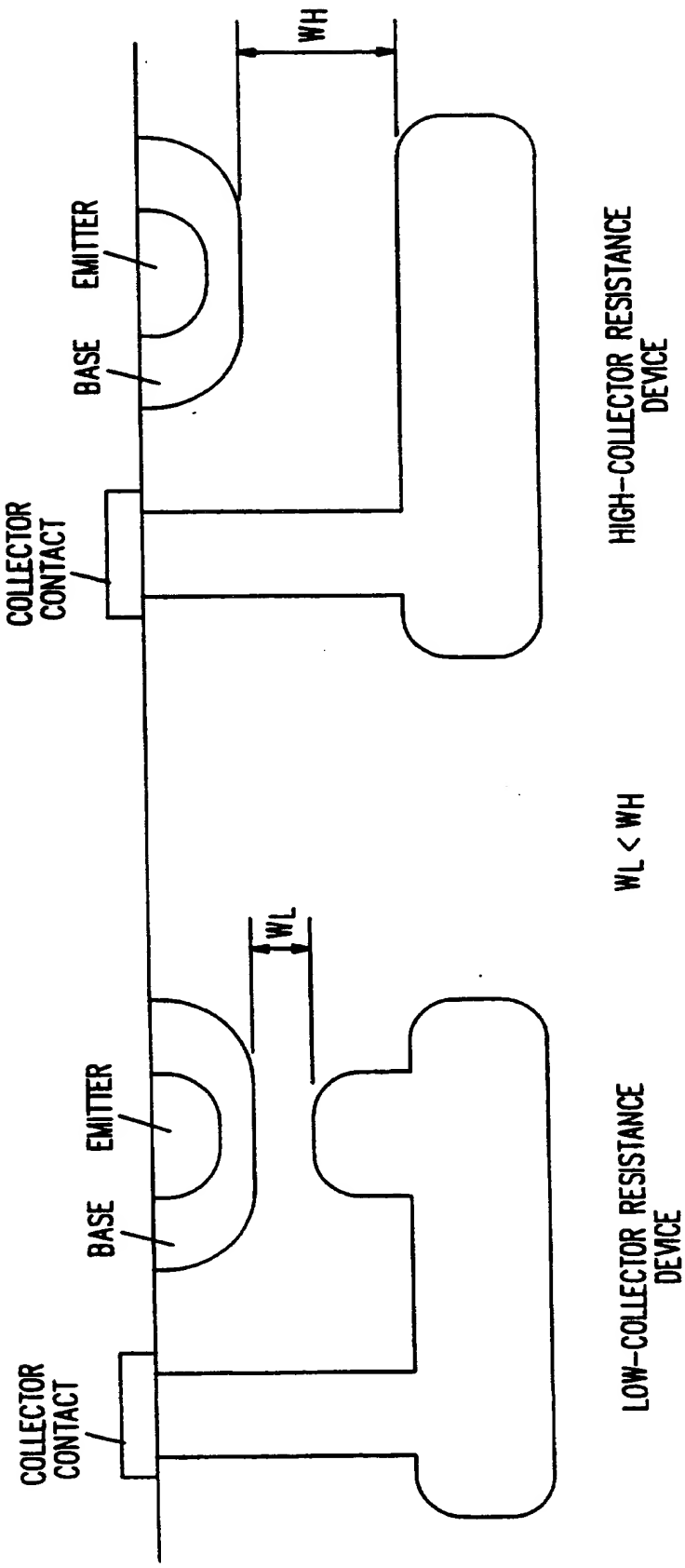

WH
EMITTER
BASE
COLLECTOR CONTACT
HIGH-COLLECTOR RESISTANCE DEVICE
WL < WH
WL
EMITTER
BASE
COLLECTOR CONTACT
LOW-COLLECTOR RESISTANCE DEVICE

FIG. 2

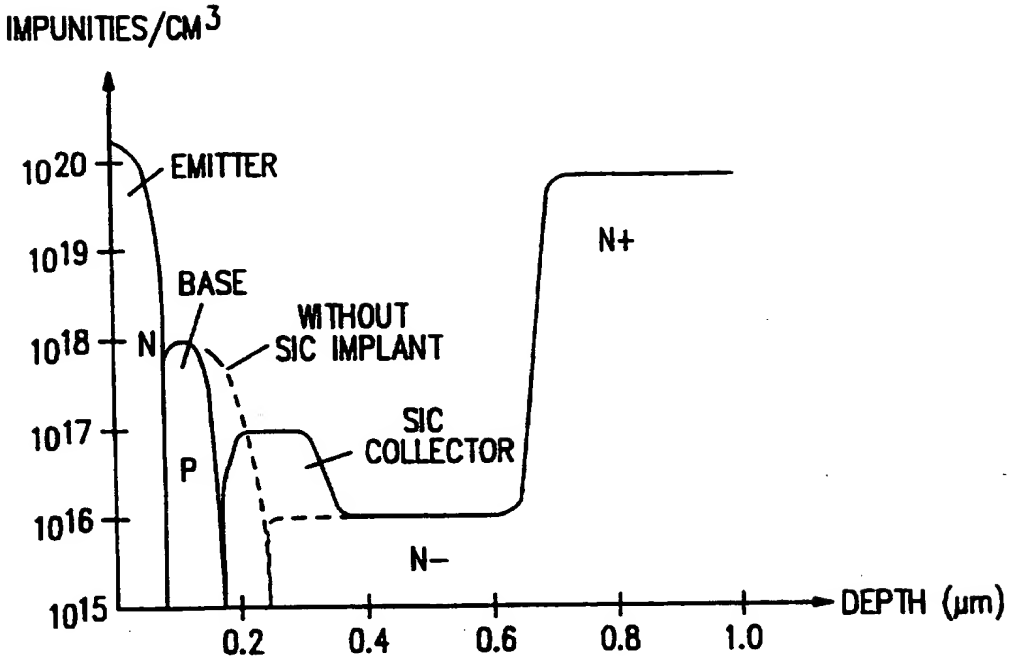
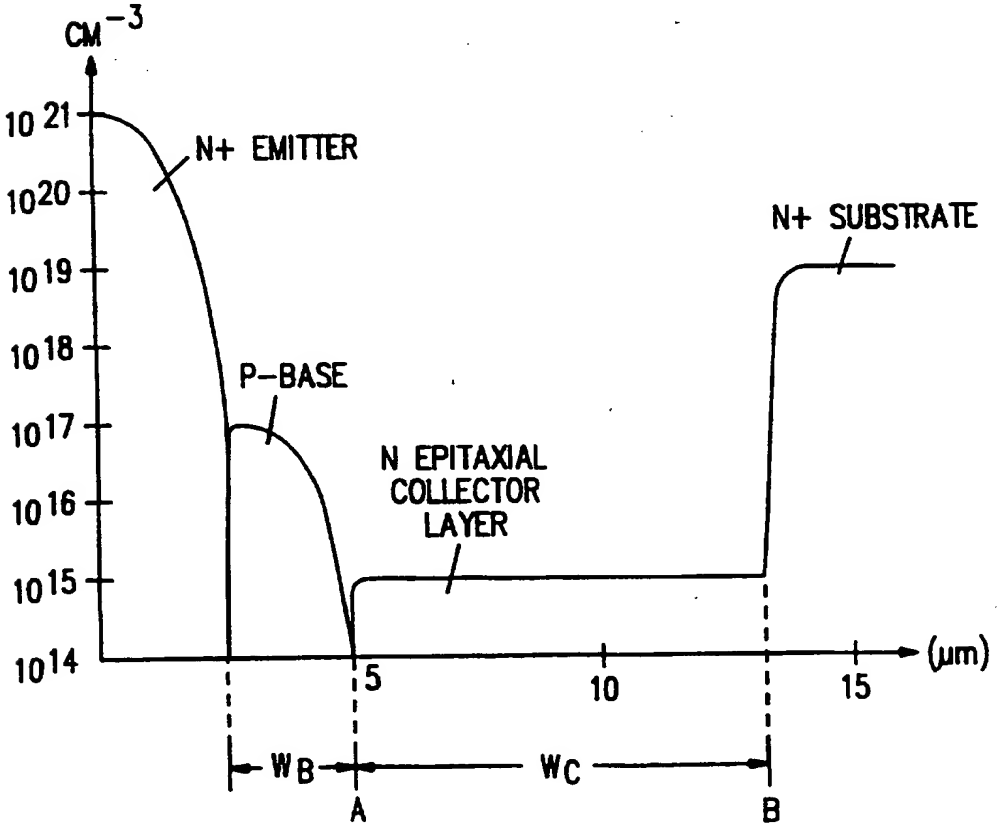
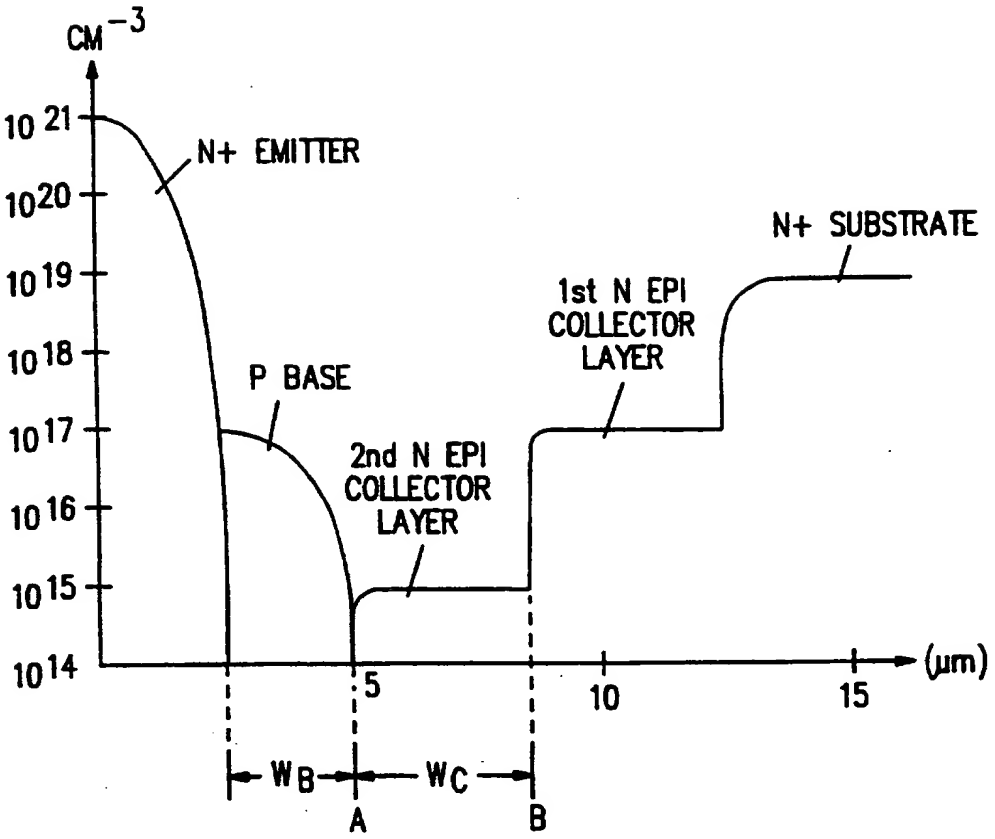


FIG. 3B



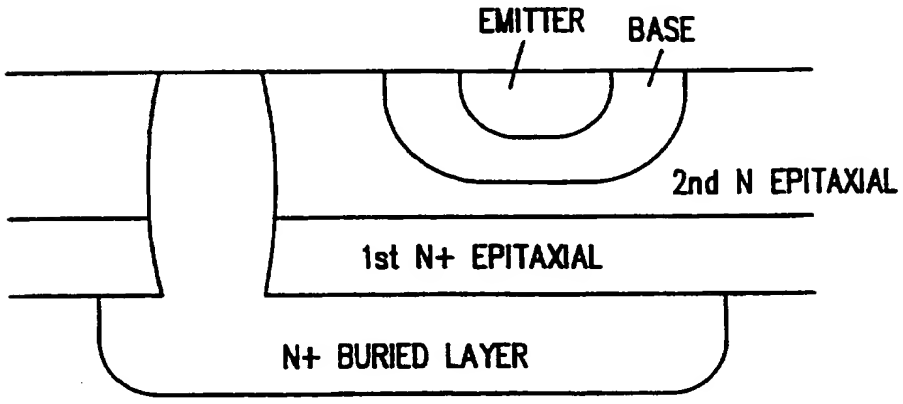
PRIOR ART

FIG. 4A



PRIOR ART

FIG. 4B



PRIOR ART

FIG. 4C

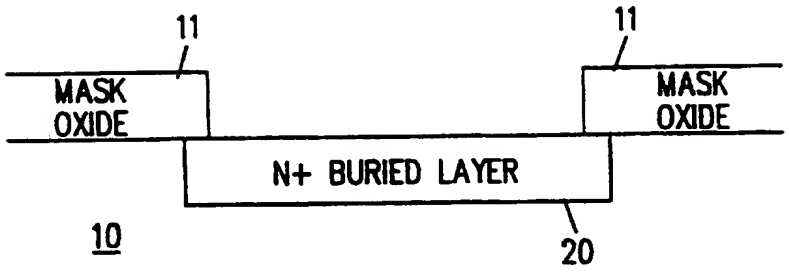


FIG. 5

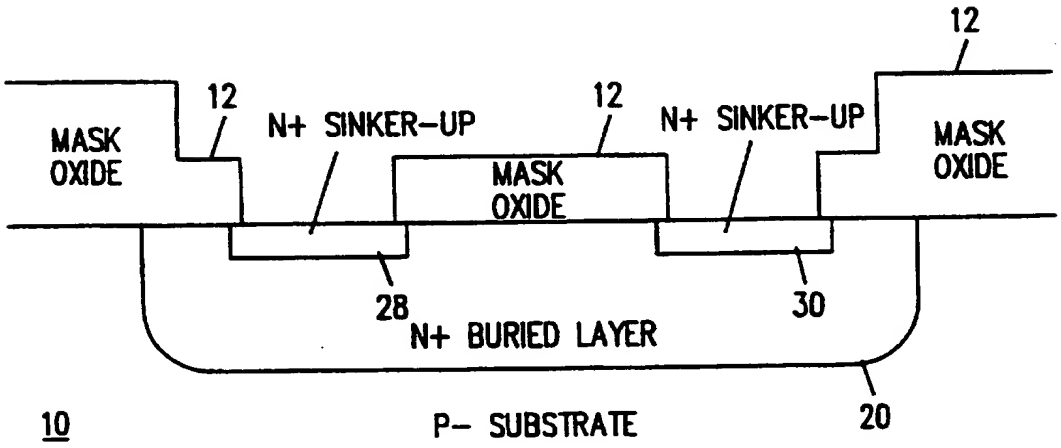


FIG. 6

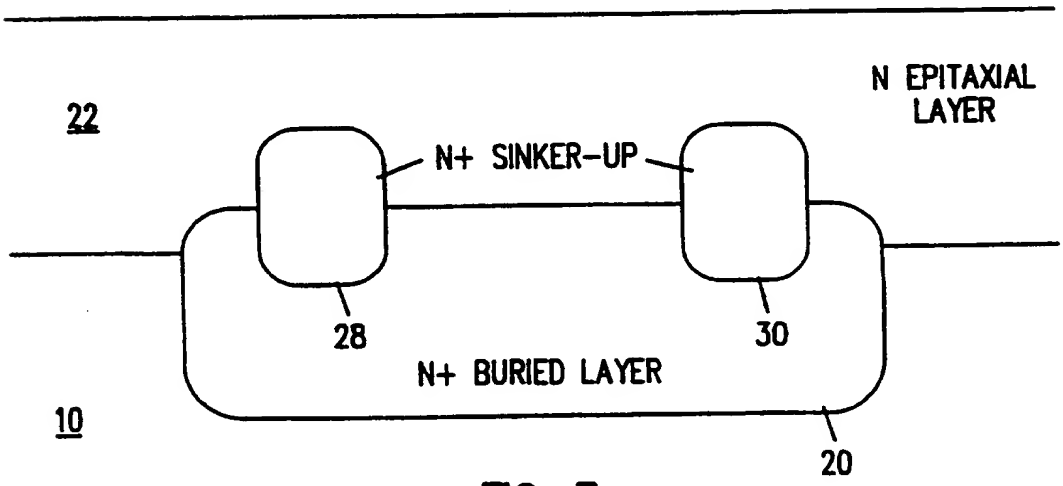


FIG. 7

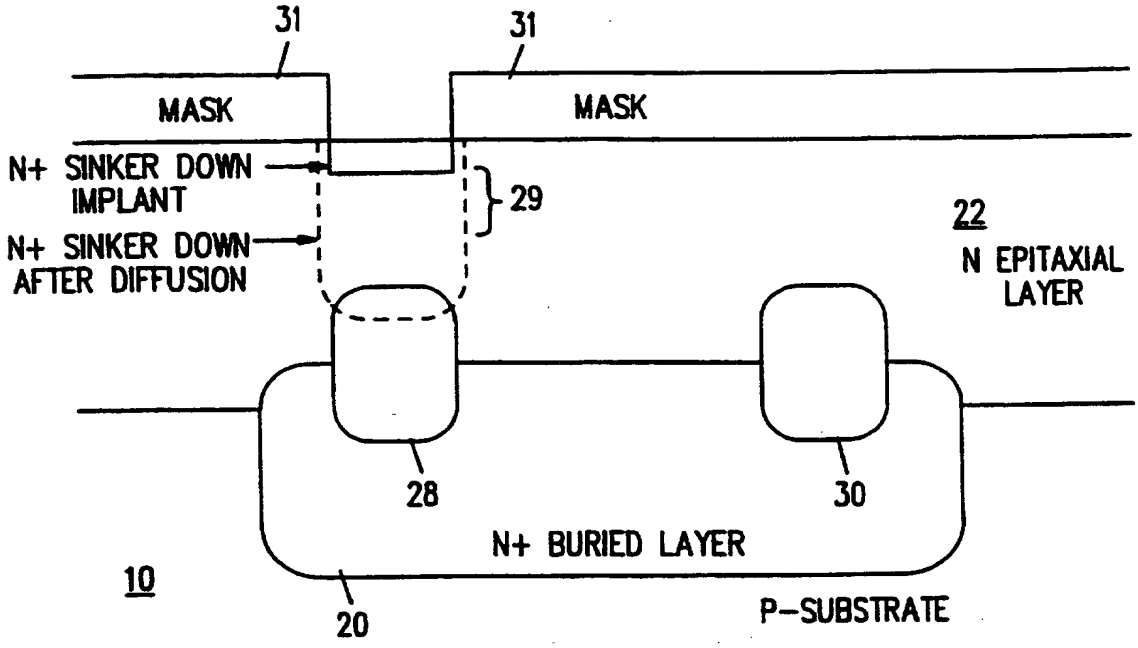

31
31
MASK
MASK
N+ SINKER DOWN IMPLANT
N+ SINKER DOWN AFTER DIFFUSION
29
22
N EPITAXIAL LAYER
28
30
N+ BURIED LAYER
10
20
P-SUBSTRATE

FIG. 8

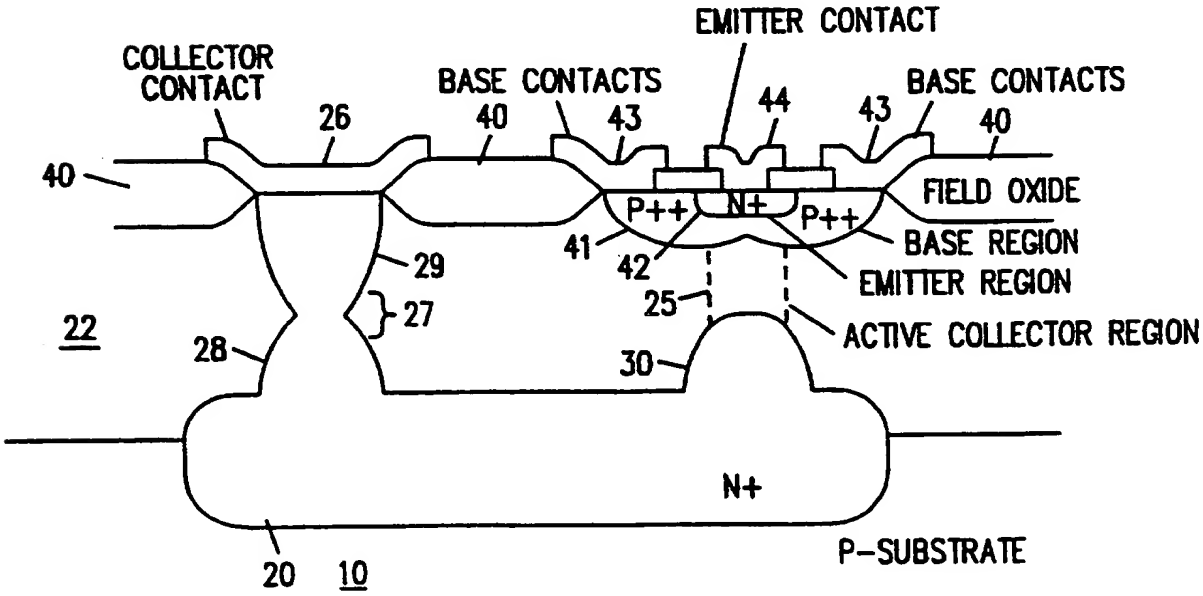

EMITTER CONTACT
COLLECTOR CONTACT
BASE CONTACTS
BASE CONTACTS
26
40
43
44
43
40
40
FIELD OXIDE
P++
N+
P++
41
42
BASE REGION
EMITTER REGION
29
27
25
22
28
30
ACTIVE COLLECTOR REGION
N+
20
10
P-SUBSTRATE

FIG. 9

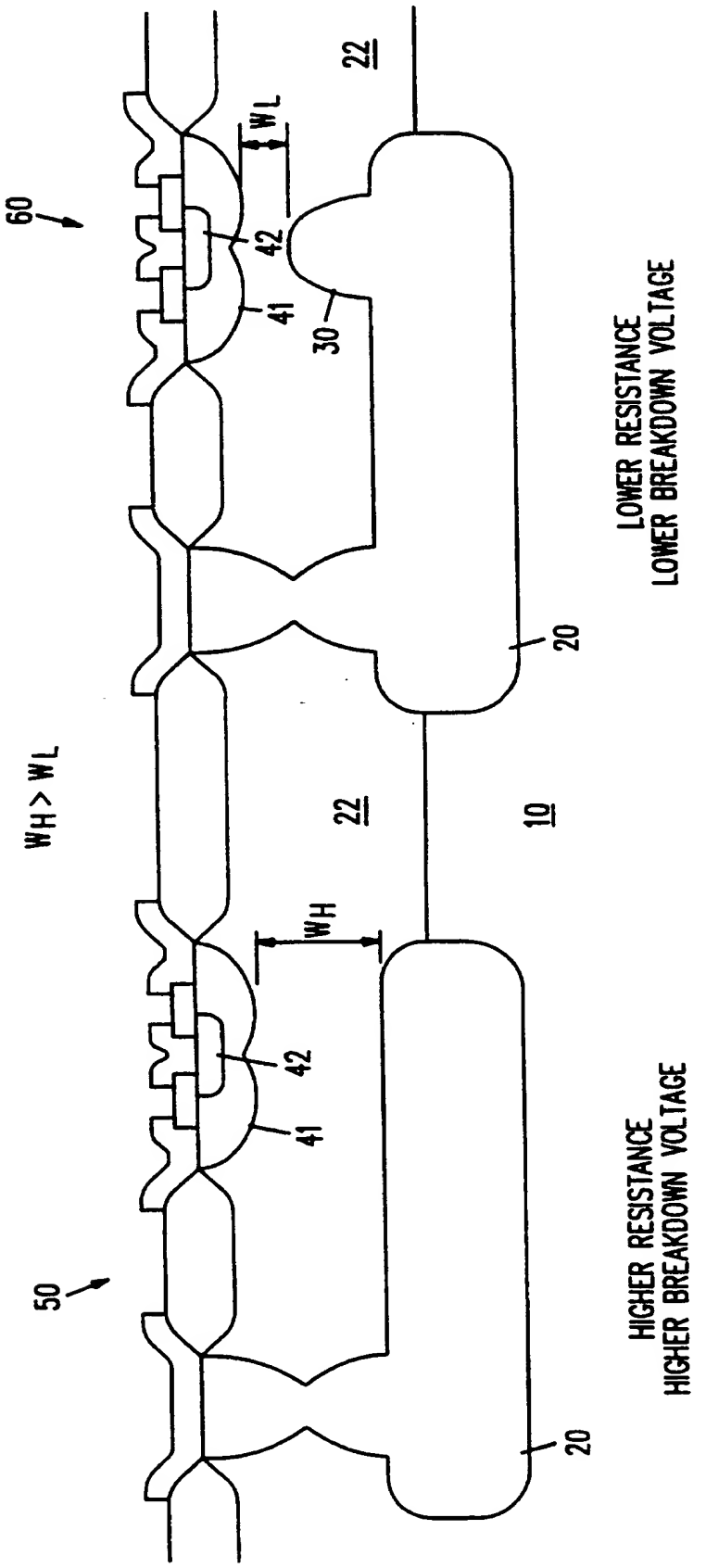

60
50
22
22
10
20
20
42
41
42
41
30
W_L
W_H
$W_H > W_L$
LOWER RESISTANCE
LOWER BREAKDOWN VOLTAGE
HIGHER RESISTANCE
HIGHER BREAKDOWN VOLTAGE

FIG. 10

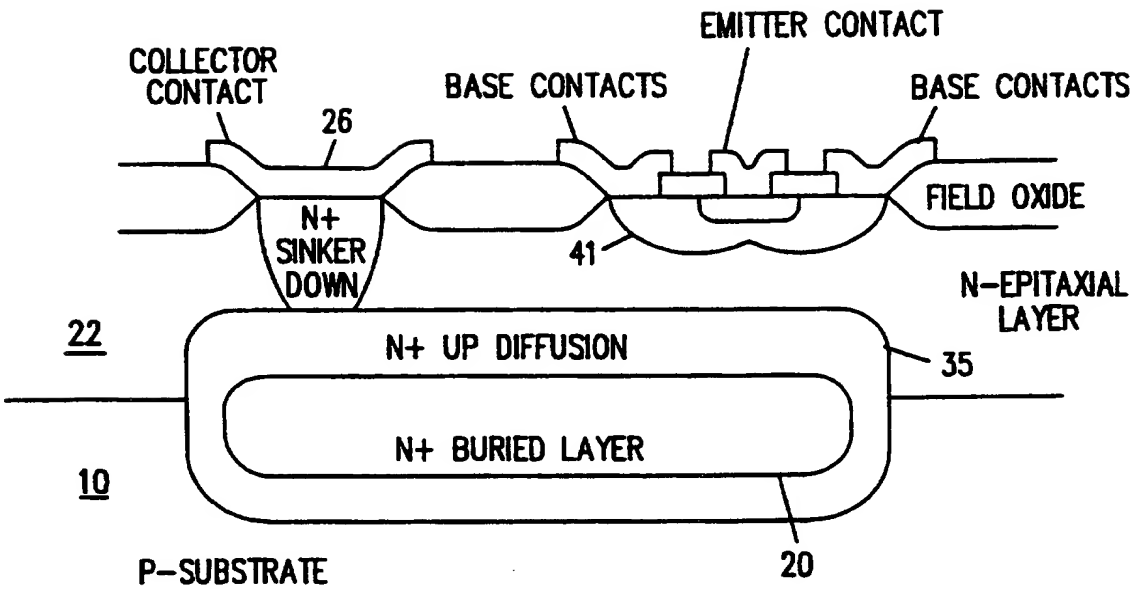

COLLECTOR CONTACT
26
BASE CONTACTS
EMITTER CONTACT
BASE CONTACTS
FIELD OXIDE
N+ SINKER DOWN
41
N-EPITAXIAL LAYER
22
N+ UP DIFFUSION
35
N+ BURIED LAYER
10
P-SUBSTRATE
20

FIG. 11

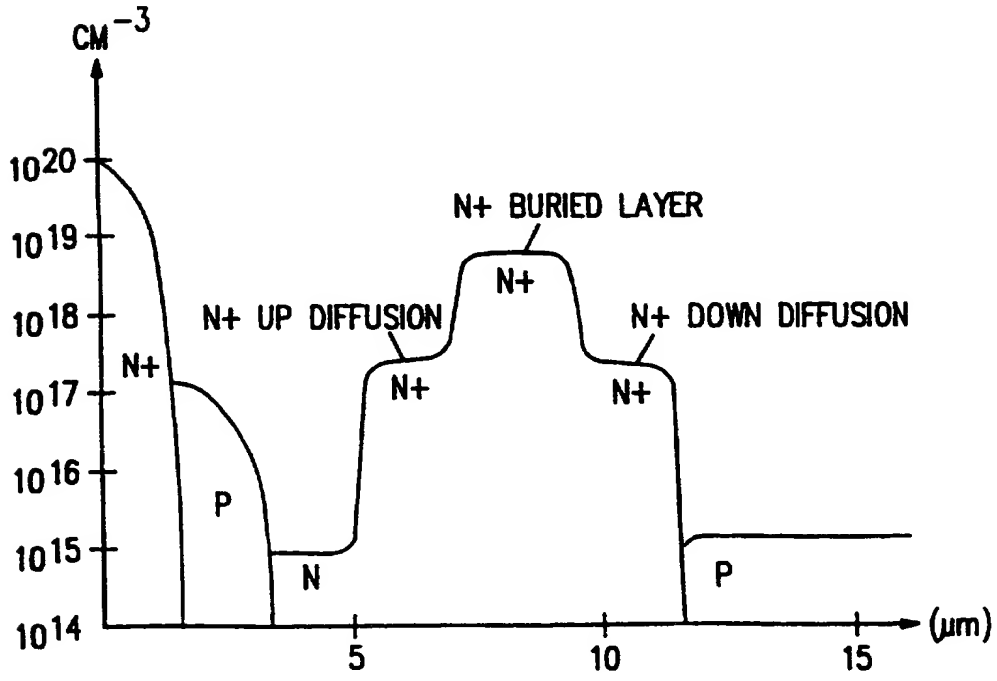

CM -3
10 20
10 19
10 18
10 17
10 16
10 15
10 14
N+ BURIED LAYER
N+
N+ UP DIFFUSION
N+ DOWN DIFFUSION
N+
N+
N+
P
N
P
5
10
15
(μm)

FIG. 12

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/US 95/12436

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/331 H01L29/732 H01L29/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 7, no. 178 (E-191), 6 August 1983 & JP,A,58 084442 (TOKYO SHIBAURA DENKI KK), 20 May 1983, see abstract ---	1,3,4,6, 7,10,12, 13,15, 16,19, 20,22,23
X	EP,A,0 500 233 (NATIONAL SEMICONDUCTOR CORPORATION) 26 August 1992 see the whole document ---	1-4,6,7, 10-13, 15,16, 19,20, 22,23
A	EP,A,0 463 745 (THE GENERAL ELECTRIC COMPANY) 2 January 1992 see the whole document --- -/--	1,5,10, 14,19,21

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 July 1996	16. 07. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Baillet, B

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INTERNATIONAL SEARCH REPORT

Interr al Application No
PCT/US 95/12436

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 5, no. 129 (E-070), 19 August 1981 & JP,A,56 066067 (PIONEER ELECTRONIC CORP), 4 June 1981, see abstract -----	1,10,19

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter nal Application No
PCT/US 95/12436

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-500233	26-08-92	JP-A- 4317369	09-11-92
EP-A-463745	02-01-92	GB-A- 2245425	02-01-92